Topology Derivation and Generalized Analysis of Zero-Voltage-Switching Synchronous DC-DC Converters with Coupled Inductors

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***Abstract*—In conventional DC-DC converters with synchronous rectifiers, hard-switching operation of the main switch and reverse-recovery problem of the synchronous switch result in degraded performance. In order to avoid these two undesired shortcomings, employing a coupled inductor is a simple yet effective solution. Apart from the improved soft-switching characteristic, low component count is also achieved since only a coupled winding and a series auxiliary diode are added. In this paper, a general zero-voltage-switching (ZVS) topology with a coupled inductor is proposed and based on which, a family of ZVS synchronous buck, boost and buck-boost converters is readily obtained. For each fundamental DC-DC converter, several viable ZVS topologies evolve, among which an optimum topology can be chosen according to the different requirement in practical engineering applications. To help the topology selection, generalized analysis and individual comparison are also undertaken. In addition, design consideration is illustrated and experiment results are provided to validate converter effectiveness. Furthermore, thanks to its generality, the topology derivation and generalized analysis can be easily extended to various synchronous DC-DC converters.**

***Index Terms*—Coupled inductor, synchronous DC-DC converters, topology derivation, zero-voltage-switching (ZVS).**

I. Introduction

DC-DC converters with synchronous rectifiers have been widely used in battery charger, solar photovoltaic application, voltage regulator module (VRM) and so on [1-4]. Replacement of the rectifier diode by a synchronous switch reduces conduction losses, and hence the overall efficiency is improved. However, performance of conventional synchronous converters is severely degraded as a result of the reverse-recovery problem suffered by the body diode of synchronous switch as analyzed in [5-8], and reference [5] incorporates an auxiliary circuit in the conventional synchronous converter to effectively eliminate the reverse-recovery problem. Besides, high switching loss caused by hard-switching operation of the main switch at high frequency further impairs converter performance. Zero-voltage-switching (ZVS) techniques including quasi-resonant (QR) ZVS [9-11], multi-resonant (MR) ZVS [12,13] and active-clamping ZVS [14-16], have been proposed to create zero-voltage turn-on condition for the main switch to achieve reduced switching loss. However, the switch is subjected to high voltage stress and conduction losses. Also, the reverse-recovery problem associated with the body diode of synchronous switch remains.

In order to achieve ZVS operation and eliminate the reverse-recovery problem simultaneously, the drain-to-source current of the synchronous switch should commute from the body diode to the switch (mosfet channel) before turn-off. The necessary current can be realized by the inductor current with large current ripple, which changes direction before the synchronous switch is turned off [17,18]. Consequently, the reverse-recovery problem is eliminated from the synchronous switch and ZVS operation of the main switch is also achieved. Moreover, the converter configuration is simple without any additional components. However, the large current ripple may cause magnetic saturation and necessitates large input and output filters. Therefore, multiphase converters are required to reduce the current ripple in each converter, but with increased system complexity. Reduced current ripple can be attained in zero-voltage-transition (ZVT) converters, which realize the desired current with an auxiliary inductor to achieve ZVS operation and eliminate the reverse-recovery problem [19-22]. Because the auxiliary circuit is removed from the main converter, conduction losses are also decreased. But the cost is increased owing to the additional auxiliary switch. Furthermore, in order to implement the auxiliary inductor, the number of magnetic core is increased, which results in higher volume.

Due to the competitive advantages of low component count and reduced current ripple, ZVS synchronous DC-DC converters with coupled inductors are attractive [5, 23-29]. In [5, 23-24], ZVS synchronous buck and boost converters with coupled inductors are proposed and analyzed, respectively. In comparison with the ZVT converters in [19-22], the additional

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magnetic core is eliminated since the leakage inductor of the coupled inductor fulfils the role of the auxiliary inductor and the magnetizing inductor functions as the converter inductor. Moreover, the auxiliary switch is replaced by a diode to reduce costs. In addition, the current ripple of magnetizing inductor is decreased when compared to the converter with large inductor current ripple in [17, 18]. However, only one specific ZVS topology is proposed for the synchronous buck or boost converters in [5, 23-24], which cannot always be the best choice in different applications. Therefore, optional topologies should be provided for engineers to make an optimum selection according to different requirements.

Based on the concept of achieving ZVS and eliminating the reverse-recovery problem with coupled inductors in [5, 23-24], the paper aims to explore a systematic methodology of topology derivation and gain a comprehensive understanding of topology relationship on the ZVS synchronous DC-DC converters with coupled inductors. First of all, a general ZVS topology based on the unified basic cell is proposed. From the general ZVS topology, various ZVS synchronous DC-DC converters with coupled inductors can be derived, including the synchronous buck, boost and buck-boost converters. Based on different connections of the coupled inductor, there are several viable ZVS topologies for each converter, including the converters proposed in [5, 23-24]. Hence, alternatives are provided and an optimum topology can be chosen according to the requirement. Furthermore, analysis based on the general ZVS topology is also presented to gain a more comprehensive and concise understanding. The steady-state characteristics including ZVS operation and reverse-recovery problem elimination are addressed in detail. As an example, the performance of ZVS synchronous buck converters are compared in terms of the soft-switching characteristics, auxiliary diode voltage stress and average magnetizing current to explore their features, which is beneficial to the better topology selection for engineers in different applications. Moreover, the topology derivation and generalized analysis based on the general ZVS topology is not limited to the synchronous buck, boost and buck-boost converters and it can revolutionize the way for many other synchronous converters which consist of the basic cell.

The paper is organized as follows. Topology derivation of ZVS synchronous buck, boost, buck-boost converters, together with the operation principle are introduced in Section II. Section III presents the generalized analysis and individual comparison. Section IV demonstrates design considerations, accompanied with experiment results to establish the effectiveness of the proposed converters. Finally, conclusions are drawn in Section V.

II. Topology Derivation and Operation Principle

In order to explore a topology derivation methodology for various synchronous DC-DC converters, a general ZVS topology based on its basic cell is proposed. From the general ZVS topology, several different topology configurations can be derived for a specific synchronous DC-DC converter. As an example, five viable ZVS synchronous buck, boost, buck-boost converters with coupled inductors are obtained for each in the section.

A. General ZVS Topology with a Coupled Inductor

The basic cell of conventional synchronous DC-DC converters is shown in Fig. 1(a), which consists of a main switch S_m with the parasitic capacitor C_{sm}, a synchronous switch S_s with the parasitic capacitor C_{ss} and an inductor L_1. With an additional coupled winding, the proposed general ZVS topology is illustrated in Fig. 1(b). The coupled inductor T_1 is modelled as an ideal transformer with turns ratio of N_p:N_s = 1:n, a magnetizing inductor L_m and a leakage inductor L_r. In order to control the leakage inductor current i_{Lr}, the coupled winding is series connected with an auxiliary diode D_a and a voltage source v_a. In comparison with ZVT converters[19-22], the additional magnetic core is eliminated because the leakage and magnetizing inductors of the coupled inductor are exploited. Moreover, the need for an additional auxiliary switch is also avoided.

The voltage source v_a can be implemented with an additional auxiliary source, but extra components are required. Benefits of reduced component and cost can be achieved from simple implementation of v_a by directly connecting its two ports p and q to two appropriate nodes among a, b, c, d in Fig. 1(b). Therefore, v_a can be derived in terms of V_x, V_y and $v_{ss}(t)$ which is the drain-to-source voltage of S_s, as shown in (1).

$$v_a(t) = k_1 V_x + k_2 V_y + k_3 v_{ss}(t) \quad (1)$$

where $k_1, k_2, k_3 \in [-1, 0, 1]$.

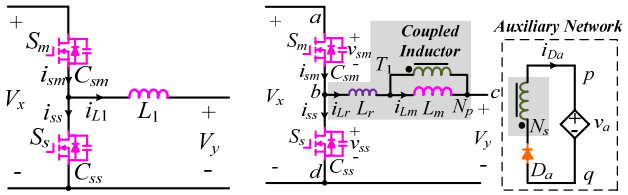

Fig. 1. Topology derivation: (a) basic cell and (b) general ZVS topology.

B. Operation Principle

To simplify the operation principle of the general ZVS topology, several assumptions are made:

—L_m is large so that the magnetizing current i_{Lm} is assumed constant,

—the leakage inductance L_r is much less than the magnetizing inductance L_m,

—the parasitic capacitances C_{sm} and C_{ss} are constant during the switching process, and their sum is denoted as C_s,

—the energy stored in the leakage inductor L_r is large enough to achieve ZVS for switches,

—all components are ideal except for the parasitic capacitances of switches.

Key operating waveforms of the general ZVS topology are shown in Fig. 2. Switches S_m and S_s are alternately operated. The operation comprises 6 stages in a switching period, and the equivalent circuits are illustrated in Fig. 3.

Prior to t_0, S_m is on and as a result of the previous stage, D_a is forward biased. The leakage inductor current i_{Lr} is increased while the auxiliary diode current i_{Da} is decreased.

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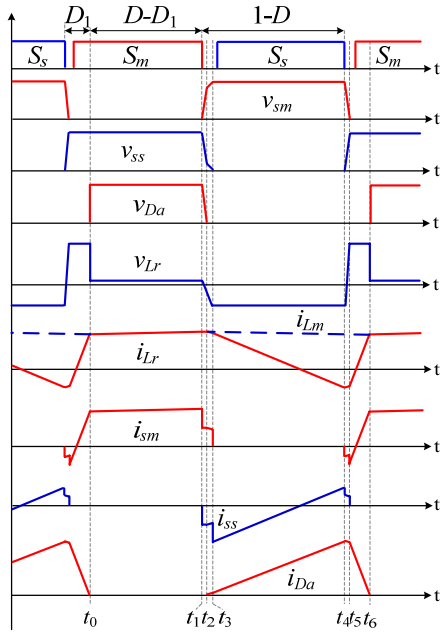

Fig. 2. Key operating waveforms.

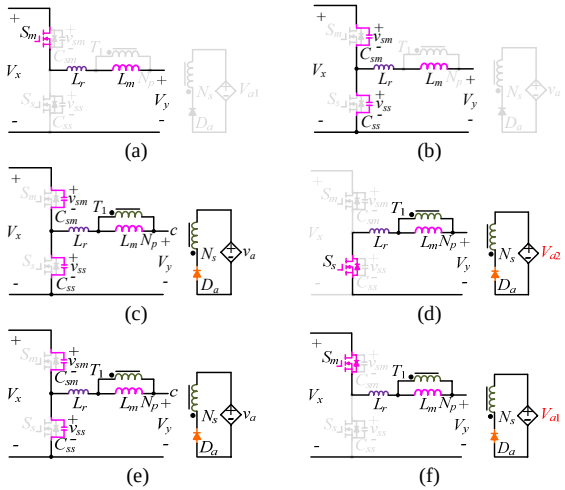

Fig. 3. Equivalent circuits of the general ZVS topology in different stages: (a) stage 1, (b) stage 2, (c) stage 3, (d) stage 4, (e) stage 5 and (f) stage 6.

Stage 1 (t_0-t_1): At t_0, i_{Da} decays to zero, thus D_a is reverse biased. In this stage, the leakage inductor L_r and the magnetizing inductor L_m are energized by V_x-V_y. With large L_m, the magnetizing current is considered constant and is denoted as I_{Lm}.

$$i_{sm}(t) = i_{Lr}(t) = i_{Lm}(t) \approx I_{Lm} \tag{2}$$

Stage 2 (t_1-t_2): S_m is turned off at t_1. The parasitic capacitor of S_m is charged and that of S_s is discharged. The drain-to-source voltage v_{ss} decreases linearly, as shown in (4). The voltage v_{Da} across D_a is derived in (5) with the neglect of leakage inductance L_r, which is assumed to be much less than the magnetizing inductance L_m. From (5), v_{Da} decreases with n+k_3>0, which can be derived from the constraint in Table I.

$$\frac{C_s}{2}\frac{dv_{ss}(t)}{dt} = i_{ss}(t) = -i_{sm}(t) = -\frac{1}{2}I_{Lm} \tag{3}$$

$$v_{ss}(t) = V_x - \frac{I_{Lm}}{C_s}(t - t_1) \tag{4}$$

$$\begin{aligned} v_{Da}(t) &= v_a(t) + n(v_{ss}(t) - V_y)\frac{L_m}{L_r + L_m} \\ &\approx k_1 V_x + (k_2 - n)V_y + (n + k_3)v_{ss}(t) \end{aligned} \tag{5}$$

Stage 3 (t_2-t_3): At t_2, v_{Da} drops to zero, hence D_a is forward biased and the diode current i_{Da} can be derived from magnetizing current I_{Lm} and leakage inductor current i_{Lr}. During this stage, the voltage of magnetizing inductance L_m is clamped to $-\frac{1}{n}v_a(t)$, and L_r resonates with C_s as illustrated in (7).

$$i_{Da}(t) = \frac{1}{n}(I_{Lm} - i_{Lr}(t)) \tag{6}$$

$$\begin{cases} L_r \dfrac{di_{Lr}(t)}{dt} = v_{ss}(t) + \dfrac{1}{n}v_a(t) - V_y \\ C_s \dfrac{dv_{ss}(t)}{dt} = k_3 i_{Da}(t) - i_{Lr}(t) \end{cases} \tag{7}$$

Stage 4 (t_3-t_4): The voltage v_{ss} decreases to zero at t_3 and current i_{ss} flows through the body diode of S_s, hence ZVS of S_s is achieved. v_a is constant in this stage and is derived in (8) from (1) with $v_{ss}(t)$=0. From Fig. 3(d), the leakage inductor voltage v_{Lr}=V_{a2}/n-V_y can be derived and the leakage inductor current i_{Lr} is decreased as illustrated in (9). From (6), the auxiliary diode current i_{Da} increases. At t_4, i_{Lr} reaches its minimum value $i_{Lr,\min}$, as illustrated in (10). In order to eliminate the reverse-recovery problem of body diode, current i_{ss} must become positive before S_s is turned off. Therefore, $i_{Lr,\min}$ is less than zero when k_3=0 or k_3=-1, and may be large than zero when k_3=1. It is noted that the operation principle is similar whether $i_{Lr,\min}$ is negative or positive and thus Fig. 2 only depicts waveforms in the condition with $i_{Lr,\min}$<0.

$$V_{a2} = k_1 V_x + k_2 V_y \tag{8}$$

$$i_{Lr}(t) = i_{Lr}(t_3) - \frac{(nV_y - V_{a2})}{nL_r}(t - t_3) \tag{9}$$

$$i_{Lr,\min} = k_3 i_{Da}(t_4) - i_{ss}(t_4) \tag{10}$$

Stage 5 (t_4-t_5): At t_4, S_s is turned off. The resonant process of L_r and C_s is similar to that in stage 3.

Stage 6 (t_5-t_6): The voltage v_{ss} is increased to V_x at t_5 and the current i_{sm} flows through the body diode of S_m, hence S_m is ZVS turned on. v_a is also constant in this stage, as derived in (11). The leakage inductor current i_{Lr} is increased while the auxiliary diode current i_{Da} is decreased. In this stage, the drain-to-source current i_{sm} changes from negative to positive. The switching period ends at t_6 when i_{Da} drops to zero.

$$V_{a1} = (k_1 + k_3)V_x + k_2 V_y \tag{11}$$

$$i_{Lr}(t) = i_{Lr}(t_5) + \frac{V_{a1} + n(V_x - V_y)}{nL_r}(t - t_5) \tag{12}$$

C.ZVS Synchronous buck, boost, buck-boost Converters

Theoretically there are $A_4^2 = 12$ different ways to implement voltage source v_a because its two ports p and q can be connected to any two nodes among a, b, c, d. However, some violate the following two constraints derived from the previous operation

principle analysis.

The first constraint is that the leakage inductor current i_{Lr} should decrease in the interval t_3-t_4 to achieve ZVS operation of S_m as well as eliminate the reverse-recovery problem of S_s, and should increase in the interval t_5-t_6 to reach the magnetizing current I_{Lm}. Therefore, the requirement in (13) derived from (9) and (12) has to be satisfied. The second constraint is that the average voltage across D_a must be larger than zero since the auxiliary diode D_a is reverse biased in the interval t_0-t_1. With these two restrictions, only five connections are feasible, which are illustrated in Table I.

$$\begin{cases} nV_y - V_{a2} > 0 \\ n(V_x - V_y) + V_{a1} > 0 \end{cases} \tag{13}$$

$$\bar{v}_{Da} = \bar{v}_a + n\bar{v}_{Lm} \approx DV_{a1} + (1-D)V_{a2} > 0 \tag{14}$$

where D is the duty-cycle of main switch S_m.

TABLE I
FIVE IMPLEMENTATIONS OF v_a

	Constraint	k_1	k_2	k_3
(p, q)-->(a, b)	$n>V_x/V_y$	1	0	-1
(p, q)-->(a, c)	$n>(V_x - V_y)/V_y$	1	-1	0
(p, q)-->(a, d)	$n>V_x/V_y$	1	0	0
(p, q)-->(b, d)	$n>0$	0	0	1
(p, q)-->(c, d)	$n>1$	0	1	0

Various ZVS synchronous DC-DC converters can be derived from the general ZVS topology, and the practical ZVS topologies of the synchronous buck, boost and buck-boost converters with different connections of ports (p, q) are respectively demonstrated in Fig. 4, Fig. 5 and Fig. 6, as an example. Several have been published while most are novel to this paper. Each implementation of v_a has its individual advantages, associated with the different applications. In the following section, ZVS synchronous buck converters in applications with different input voltage will be compared.

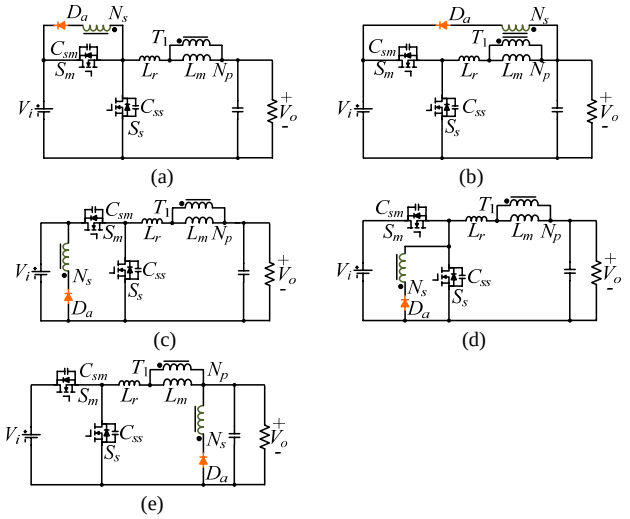

Fig. 4. ZVS synchronous buck converters with different connections of (p, q): (a) (a, b), (b) (a, c), (c) (a, d), (d) (b, d)[5] and (e) (c, d).

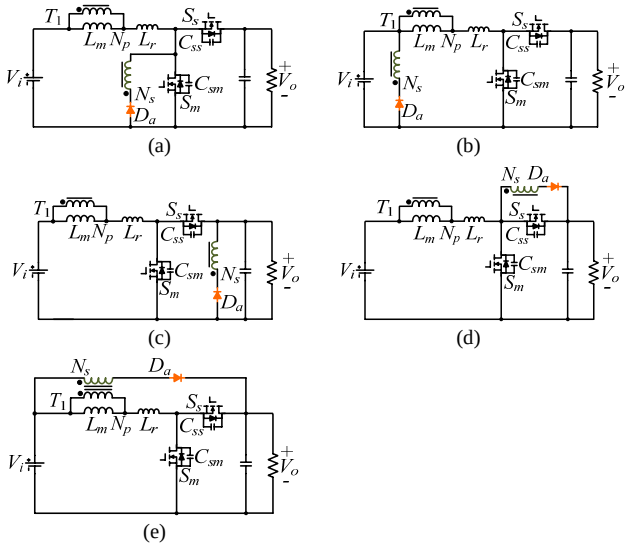

Fig. 5. ZVS synchronous boost converters with different connections of (p, q): (a) (a, b), (b) (a, c), (c) (a, d), (d) (b, d)[23-24] and (e) (c, d).

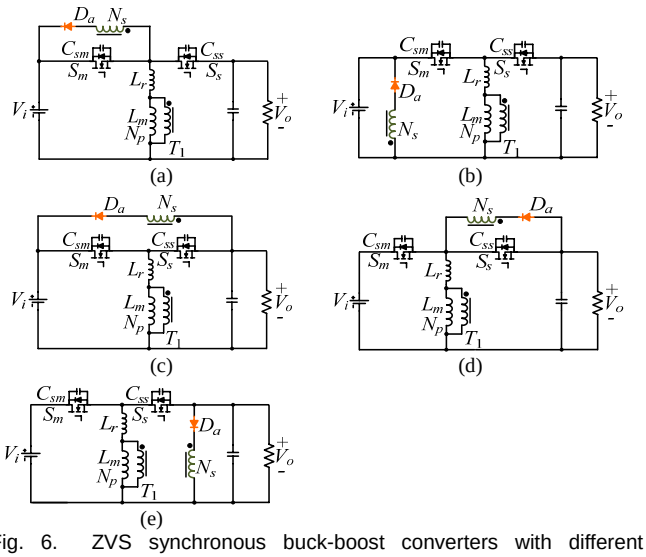

Fig. 6. ZVS synchronous buck-boost converters with different connections of (p, q): (a) (a, b), (b) (a, c), (c) (a, d), (d) (b, d) and (e) (c, d).

III. GENERALIZED ANALYSIS

Generalized analysis of all ZVS synchronous buck, boost and buck-boost converters in Fig. 4-Fig. 6 is performed. The steady-state characteristics are presented in detail with the neglect of dead-time which is relatively short. Also, the requirements for achieving ZVS and eliminating the reverse-recovery problem are derived. Thanks to the unity of analysis, comprehensive understanding of these converters is obtained and individual comparison can be readily conducted to explore their correspondingly preferred applications.

A. Voltage Transfer Ratio

The average voltage across leakage inductor and magnetizing inductor in a switching period is zero owing to the flux balance. Therefore, assuming the dead-time is insignificant, the voltage transfer ratio of ZVS synchronous buck, boost and buck-boost converters is given in (15), which is the same as that

of conventional converters.

$$M(D)=\frac{V_o}{V_i}=\begin{cases}D, & \text{buck}\\ \dfrac{1}{1-D}, & \text{boost}\\ -\dfrac{D}{1-D}, & \text{buck-boost}\end{cases} \quad (15)$$

B. Auxiliary Diode Current Reset Time

The auxiliary diode current is reset from the maximum to zero and the leakage inductor current increases from $i_{Lr,\min}$ to I_{Lm} in the interval t_5-t_6, which is denoted as D_1T. The change in i_{Lr} is given in (16) and thus D_1 and $i_{Lr,\min}$ can be derived.

$$\Delta i_{Lr}=\frac{n(V_x-V_y)+V_{a1}}{nL_r}D_1T\approx\frac{nV_y-V_{a2}}{nL_r}(1-D)T \quad (16)$$

$$D_1=\frac{nV_y-V_{a2}}{n(V_x-V_y)+V_{a1}}(1-D) \quad (17)$$

$$i_{Lr,\min}=I_{Lm}-\Delta i_{Lr}=I_{Lm}-\frac{nV_y-V_{a2}}{nL_r}(1-D)T \quad (18)$$

C. Voltage and Current Stress of Switches

The turn-off voltage of switches S_m and S_s in the proposed ZVS converters is clamped, as with the corresponding conventional converters. The current stress of switches can be easily derived from Fig. 2.

$$I_{sm,rms}\approx\sqrt{\frac{D_1}{3}(i_{sm}^2(t_5)+i_{sm}(t_5)I_{Lm}+I_{Lm}^2)+(D-D_1)I_{Lm}^2} \quad (19)$$

$$I_{ss,rms}\approx\sqrt{\frac{1-D}{3}(i_{ss}^2(t_4)-i_{ss}(t_4)I_{Lm}+I_{Lm}^2)} \quad (20)$$

where $i_{sm}(t_5)\approx -i_{ss}(t_4)=\dfrac{n+k_3}{n}i_{Lr,\min}-\dfrac{k_3}{n}I_{Lm}$.

D. Voltage and Current Stress of Diode D_a

The auxiliary diode D_a is reverse biased in the interval t_0-t_1, and the turn-off voltage is given in (21). Maximum current $i_{Da,\max}$ is achieved at t_4 as illustrated in (22). Then the average diode current I_{Da} can be derived.

$$V_{Da}=\frac{L_m}{L_r+L_m}n(V_x-V_y)+V_{a1}\approx n(V_x-V_y)+V_{a1} \quad (21)$$

$$i_{Da,\max}=\frac{1}{n}\Delta i_{Lr}=\frac{nV_y-V_{a2}}{n^2L_r}(1-D)T \quad (22)$$

$$\begin{aligned}I_{Da}&=\frac{1}{2}(1-D+D_1)i_{Da,\max}\\&=\frac{(1-D)^2T}{2n^2L_r}\frac{nV_x+V_{a1}-V_{a2}}{n(V_x-V_y)+V_{a1}}(nV_y-V_{a2})\end{aligned} \quad (23)$$

E. Average Magnetizing Current I_{Lm} and Magnetizing Inductance L_m

The average leakage inductor current of the ZVS synchronous buck converters shown in Fig. 4 is given in (24). Therefore, the average magnetizing current I_{Lm} in ZVS synchronous buck converters is derived in (25). Likewise, I_{Lm} in ZVS synchronous boost and buck-boost converters also can be obtained in (26) and (27), respectively.

$$I_{Lr,buck}=-k_2I_{Da}+I_o \quad (24)$$

$$I_{Lm,buck}=I_{Lr,buck}+nI_{Da}=(n-k_2)I_{Da}+I_o \quad (25)$$

$$I_{Lm,boost}=(n-k_2)I_{Da}+I_i \quad (26)$$

$$I_{Lm,buck-boost}=(n-k_2)I_{Da}+I_i+I_o \quad (27)$$

where I_i and I_o is the average input current and output current, respectively.

According to Fig. 2, the magnetizing inductance is charged by V_x-V_y in the interval [t_0, t_1]. Then the required magnetizing inductance in terms of the magnetizing current ripple is derived in (28).

$$L_m=\frac{(D-D_1)(V_x-V_y)T_s}{\Delta I_{Lm}} \quad (28)$$

F. Analysis of ZVS Operation and Reverse-Recovery Problem Elimination

The ZVS turn-on process of S_s is divided into two intervals, t_1-t_2 and t_2-t_3. In the interval t_1-t_2 as shown in Fig. 3 (b), the parasitic capacitance of S_s is discharged by L_r and L_m. Since L_m is large enough to maintain constant current, the drain-to-source voltage v_{ss} is almost linearly decreased until t=t_2 when the auxiliary diode D_a is forward biased and v_{ss} drops to V_{com} in (29). In the interval t_2-t_3 as illustrated in Fig. 3 (c), the voltage of L_m is clamped by $-v_a(t)/n$, and L_r resonates with C_s as illustrated in (7). The voltage v_{ss} in the resonant process is derived in (30) with $v_{ss}(t_2)=V_{com}$ and $i_{Lr}(t_2)=I_{Lm}$. In order to achieve ZVS of S_s, $V_{com}-I_{Lm}/(\omega C_s)$ should be less than zero. The ZVS condition is given in (31). It can be inferred that the ZVS of S_s is easier to be realized with a larger I_{Lm}. Hence the ZVS can be achieved over the whole load range when (31) is guaranteed at a no load condition.

$$v_{ss}(t_2)=-\frac{k_1}{n+k_3}V_x+\frac{n-k_2}{n+k_3}V_y=V_{com} \quad (29)$$

$$v_{ss}(t)=V_{com}-\frac{I_{Lm}}{\omega C_s}\sin\omega(t-t_2) \quad (30)$$

$$Z_1=(\frac{n}{n+k_3})^2L_rI_{Lm}^2-C_sV_{com}^2>0 \quad (31)$$

where $\omega=\dfrac{n+k_3}{n}\dfrac{1}{\sqrt{L_rC_s}}$.

The ZVS turn-on process of S_m in interval t_4-t_5 is similar to that of interval t_2-t_3 except with a different initial leakage inductor current $i_{Lr}(t_4)$=$i_{Lr,\min}$ and drain-to-voltage $v_{ss}(t_4)$=0. Similarly, the voltage v_{ss} can be derived. In order to achieve ZVS of S_m, $V_{com}+A_1$ should be larger than V_x and the requirement is expressed in (33).

$$v_{ss}(t)=V_{com}+A_1\sin(\omega(t-t_4)+\varphi) \quad (32)$$

$$Z_2=L_r(\Delta i_{Lr}-\frac{n}{n+k_3}I_{Lm})^2-C_s((V_x-V_{com})^2-V_{com}^2)>0 \quad (33)$$

where $A_1=\sqrt{V_{com}^2+\dfrac{L_r}{C_s}(\dfrac{k_3}{n+k_3}I_{Lm}-i_{Lr,\min})^2}$,

$$\varphi = \arctan\sqrt{\frac{C_s}{L_r}}\frac{V_{com}}{i_{Lr,\min} - k_3 I_{Lm}/(n+k_3)}.$$

In order to eliminate the reverse-recovery problem suffered by the body diode of the synchronous switch S_s, the drain-to-source current i_{ss} should turn to positive before S_s is turned off at t_4.

$$i_{ss}(t_4) = \frac{n+k_3}{n}\Delta i_{Lr} - I_{Lm} > 0 \qquad (34)$$

From (33) and (34), ZVS of the main switch S_m and reverse-recovery problem elimination of the synchronous switch S_s could be achieved over the whole load range provided it is realized under a full-load condition.

G. Comparison

Five feasible ZVS synchronous buck, boost and buck-boost converters with coupled inductors are derived in section II. Each converter has its individual feature. Thanks to the generalized analysis, the comparison can be easily conducted, which is beneficial for engineers to select topology in practical design. Taking the ZVS synchronous buck converters in Fig. 4 as an example, converter merits including soft-switching characteristics, auxiliary diode voltage stress and average magnetizing current which is the dominant factor of the current stress of switches, are respectively demonstrated in Fig. 7, Fig. 8 and Fig. 9 at different input voltages. The converter parameters are listed: the output voltage V_o=24V, the maximum power $P_{o,max}$=115.2 W, the switching frequency f_s=100 kHz, parasitic capacitances C_s=1200 pF.

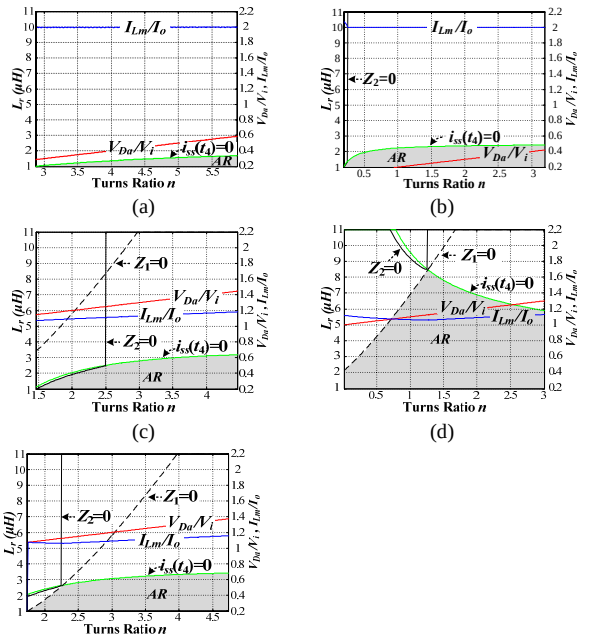

Fig. 7. Merits of ZVS synchronous buck converters at D=0.9 for different connections of (p, q): (a) (a, b), (b) (a, c), (c) (a, d), (d) (b, d) and (e) (c, d).

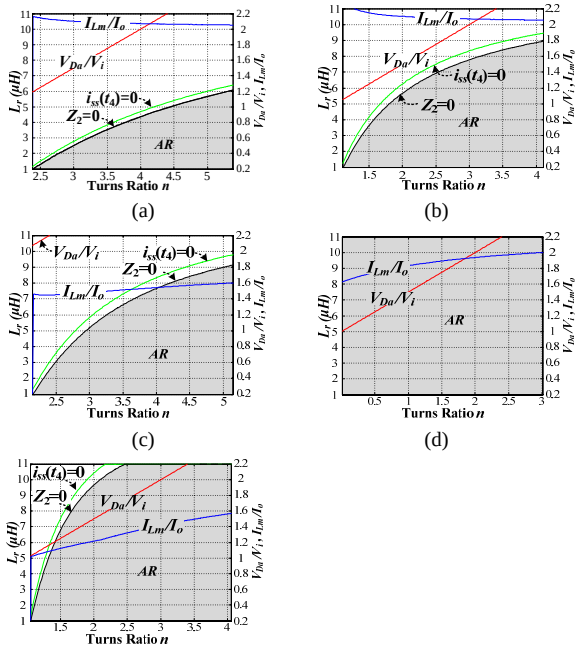

Fig. 8. Merits of ZVS synchronous buck converters at D=0.5 for different connections of (p, q): (a) (a, b), (b) (a, c), (c) (a, d), (d) (b, d) and (e) (c, d).

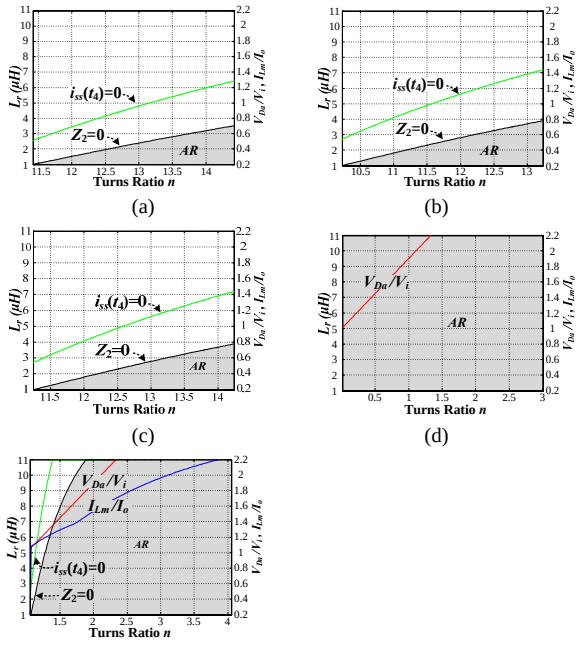

Fig. 9. Merits of ZVS synchronous buck converters at D=0.1 for different connections of (p, q): (a) (a, b), (b) (a, c), (c) (a, d), (d) (b, d) and (e) (c, d).

The available region(AR) for achieving ZVS and eliminating the reverse-recovery problem over the whole load range as a function of turns ratio n and leakage inductance L_r is depicted in Fig. 7 with duty-cycle D=0.9 for each converter according to (31), (33) and (34). Furthermore, the normalized voltage stress of auxiliary diode V_{Da}/V_i and minimum average magnetizing current I_{Lm}/I_o in the available region as a function of turns ratio n, are also illustrated. The comparison results are summarized

in Table II. The available region is larger in Fig. 7(d) than in the others. The converters in Fig. 4 (a)-(b) show advantages in terms of diode voltage stress V_{Da} as shown in Fig. 7 (a)-(b) while converters in Fig. 4 (c)-(e) achieve lower average magnetizing current I_{Lm} as illustrated in Fig. 7(c)-(e). Therefore, the preferred converter can be chosen according to the practical design requirement. Likewise, conclusions can be drawn in Table II from Fig. 8 and Fig. 9 at D=0.5 and D=0.1. It is noteworthy that V_{Da}/V_i and I_{Lm}/I_o are very large in converters in Fig. 4(a)-(c) at D=0.1, and exceeds the range as shown in Fig. 9 (a)-(c).

TABLE II
COMPARISON RESULTS OF ZVS SYNCHRONOUS BUCK CONVERTERS WITH COUPLED INDUCTORS (OUTPUT VOLTAGE V_o=24 V)

	***D*=0.9 (Fig. 7)**					***D*=0.5 (Fig. 8)**					***D*=0.1 (Fig. 9)**				
	a	***b***	***c***	***d***	***e***	***a***	***b***	***c***	***d***	***e***	***a***	***b***	***c***	***d***	***e***
AR	S	S	S	L	S	M	M	M	L	L	S	S	S	L	L
V_{Da}/V_i	S	S	M	M	M	M	M	L	M	M	L	L	L	M	M
I_{Lm}/I_o	M	M	S	S	S	M	M	M	M	S	L	L	L	L	M

Note: "S", "M" and "L" denotes "small", "medium" and "large", respectively.

From Table II, the preferred applications can be summarized for the five ZVS synchronous buck converters. The converters in Fig. 4(a)-(c) are more suitable in the applications with a large duty-cycle D. With the decrease of D, the required turns ratio n increases, which results in high voltage stress on auxiliary diode D_a. The available region(AR) of the converter in Fig. 4(d) is always large, which is preferred when achieving ZVS and eliminating reverse-recovery problem is the main focus. In the application with a low duty-cycle D, the converter in Fig. 4(e) is attractive since relatively low V_{Da} and I_{Lm} can be achieved along with a relatively large available region. Besides, this converter appears as an optimal choice for wide input voltage range applications with overall performance consideration.

The comparison results between the proposed and other ZVS buck converters are also illustrated in Table III. The QRC buck converter in [10] is very simple but with disadvantage of excessively high voltage stress on main switch. With the active-clamping circuit, the voltage stress is reduced in the active-clamping buck converter in [16], but still higher than the input voltage V_i. Moreover, both the QRC converter and the active-clamping converter are not suitable for the synchronous rectifier applications since the reverse-recovery problem remains. ZVS realization as well as reverse-recovery problem elimination are simultaneously achieved in the ZVT buck converter[19] and in the buck converter with large current ripple[18]. However, an auxiliary switch and an auxiliary magnetic core are demanded in the ZVT converter, resulting in increased cost. And large magnetic core is required for the converter in [18] since the magnetizing current ripple is large. In the proposed ZVS synchronous buck converter, the voltage stress of both main and synchronous switch is the input voltage V_i. ZVS is achieved for the main switch and reverse-recovery problem of the synchronous switch is eliminated with the coupled inductors. No additional magnetic core is needed and the magnetizing current ripple is small.

TABLE III
COMPARISON OF THE PROPOSED ZVS BUCK CONVERTER AND OTHER ZVS BUCK CONVERTERS

	Main Switch		**Reverse-Recovery Problem**	**Auxiliary Switch**	**Magnetic Component**	**Magnetizing Current Ripple**
	Voltage Stress	**ZVS**				
QRC [10]	$V_i + I_o\sqrt{L_r / C_{ds}}$	Yes	Yes	0	2	Small
Active-Clamping [16]	$V_i + 2L_r I_o / ((1-D)T_s)$	Yes	Yes	1	2	Small
ZVT [19]	V_i	Yes	No	1	2	Small
Large Current Ripple [18]	V_i	Yes	No	0	1	Large
Proposed	V_i	Yes	No	0	1	Small

IV. DESIGN CONSIDERATIONS AND EXPERIMENT VERIFICATION

A prototype circuit based on the parameters specification in section III is built to assess the presented analysis and the effectiveness of the derived topology. With input voltage V_i=48 V, the ZVS synchronous buck converter with (p, q) connected to (c, d) in Fig. 4(e) is chosen due to its excellent performance from the comparison results as illustrated in Fig. 8. Owing to its relatively lower magnetizing current I_{Lm} and voltage stress V_{Da}, reduced conduction loss and cost can be achieved.

A. Design Considerations

As for the ZVS synchronous buck converter, V_x=V_i and V_y=V_o. Meanwhile, n>1, k_1=k_3=0 and k_2=1 is acquired from Table I for the converter in Fig. 4(e). Therefore, V_{a1}=V_{a2}=V_o can be derived from (8) and (11). With these parameters, the steady-state characteristics and ZVS condition of the converter are considered in detail to achieve a better design. The duty-cycle D=0.5 can be obtained from (15) and the reset interval D_1=0.083 is calculated according to (17).

The turn-off voltage of the auxiliary diode V_{Da} is re-expressed in (35), which is linearly increased with the increment of turns ratio n. Therefore, n should be designed as small as possible to achieve low voltage stress on the auxiliary diode D_a.

$$V_{Da} = V_o + n(V_i - V_o) \tag{35}$$

The average auxiliary diode current I_{Da} and the average magnetizing current I_{Lm} can be derived from (23) and (25) respectively and are depicted in Fig. 10 as a function of leakage inductance L_r and turns ratio n. I_{Da} and I_{Lm} are lower with larger L_r and smaller n. Therefore, in order to achieve low current stress along with low conduction losses, large L_r and small n is preferred.

$$I_{Da} = \frac{(1-D)^2 T}{2nL_r} \frac{(n-1)V_i V_o}{nV_i - (n-1)V_o} \tag{36}$$

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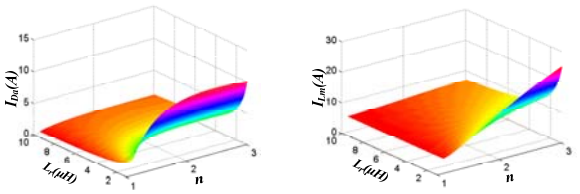
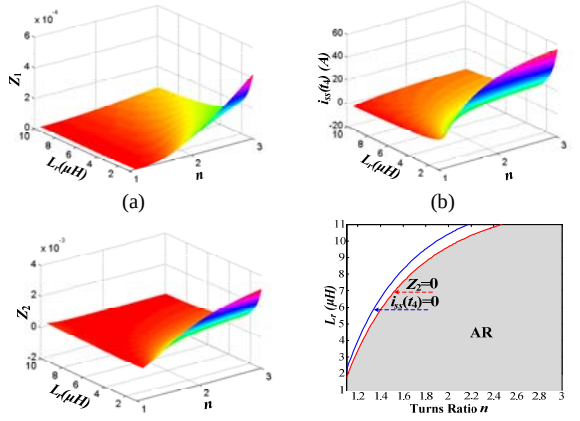
$$I_{Lm} = I_o + \frac{(1-D)^2 T}{2nL_r} \frac{(n-1)^2 V_i V_o}{nV_i - (n-1)V_o} \quad (37)$$



(a) (b)

Fig. 10. Average auxiliary diode current I_{Da} and average magnetizing current I_{Lm} as a function of the leakage inductance L_r and turns ratio n: (a) I_{Da} and (b) I_{Lm}.

The available region for achieving ZVS and eliminating the reverse-recovery problem is determined by Z_1, $i_{ss}(t_4)$ and Z_2 in (31), (33) and (34) respectively, which are depicted in Fig. 11 as a function of leakage inductance L_r and turns ratio n. Z_1, $i_{ss}(t_4)$ and Z_2 all increase as L_r decreases or n increases, and the available region is obtained in Fig. 11 (d).



(a) (b) (c) (d)

Fig. 11. The relationship of Z_1, $i_{ss}(t_4)$, Z_2 and available region with the leakage inductance L_r as well as the turns ratio n: (a) Z_1, (b) $i_{ss}(t_4)$, (c) Z_2 and (d) available region.

From above, the value of L_r and n should be chosen near the left boundary of the available region in Fig. 11 (d) to achieve ZVS as well as smaller voltage/current stress. For the coupled inductor in the experiment, ferrite core EE42 is used as the magnetic core. The number of turns for the primary and secondary windings are 23 and 32 respectively, and thus the turns ratio n is equal to1.391. The magnetizing inductance is designed as 200 μH and the leakage inductance L_r=4.46 μH is measured. The value of L_r and n is located in the AR and is close to the boundary in Fig. 11 (d). Other topology parameters can be derived from previous generalized analysis: mosfet IPP530N15N3 is chosen as switches S_m~S_s; MBR20200CT is chosen as the auxiliary diode D_a.

B. Experiment Verification

The steady-state waveforms of leakage inductor current i_{Lr}, auxiliary diode current i_{Da}, output current i_o= i_{Lr} + i_{Da} and diode voltage v_{Da} at full-load condition are shown in Fig. 12, which are in well coincidence with the presented analysis. Compared with the ZVS buck converter with a small inductor [17,18], the output current ripple is much decreased. Besides, ZVS operation is achieved by both S_m and S_s over the whole load range as illustrated in Fig. 13 and Fig. 14. S_m achieves ZVS more readily under light load condition from Fig. 13, while ZVS of S_s is more readily realized at full load, as illustrated in Fig. 14. This agrees well with the analysis in section III. Furthermore, the reverse-recovery problem is eliminated since drain-to-source current i_{sm} and i_{ss} are positive before turn-off. Therefore, the switching loss and EMI noise can be significantly reduced.

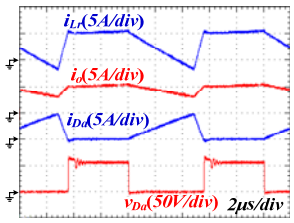
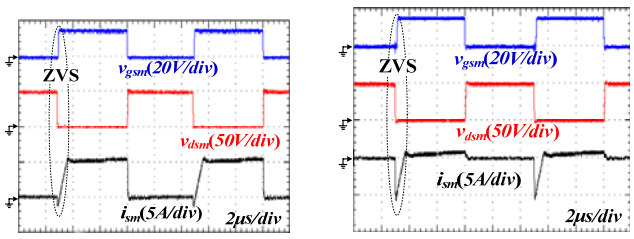
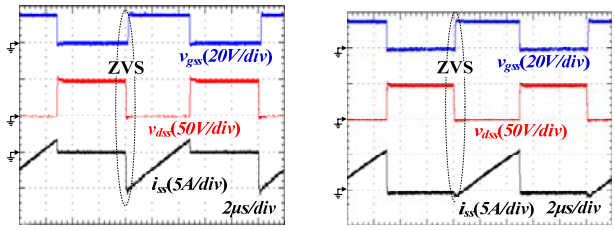


Fig. 12. Waveforms of leakage inductor current i_{Lr} , output current i_o, auxiliary diode current i_{Da} and voltage v_{Da} of the proposed ZVS buck converter at full load condition.



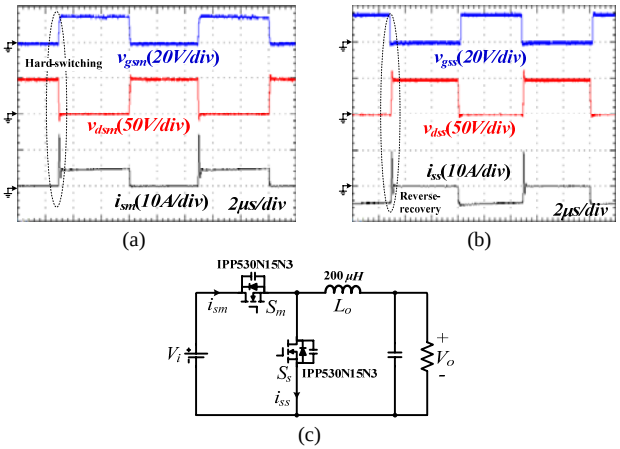
(a) (b)

Fig. 13. Waveforms of drive signal v_{gsm}, drain-to-source voltage v_{dsm} and current i_{sm} of the proposed ZVS buck converter at different load condition: (a) $P_{o,max}$ and (b) 0.01 $P_{o,max}$.



(a) (b)

Fig. 14. Waveforms of drive signal v_{gss}, drain-to-source voltage v_{dss} and current i_{ss} of the proposed ZVS buck converter at different load condition: (a) $P_{o,max}$ and (b) 0.01 $P_{o,max}$.



(a) (b) (c)

Fig. 15. Waveforms and circuit schematic of the conventional synchronous buck converter: (a) waveforms of main switch S_m, (b) waveforms of synchronous switch S_s and (c) circuit schematic.

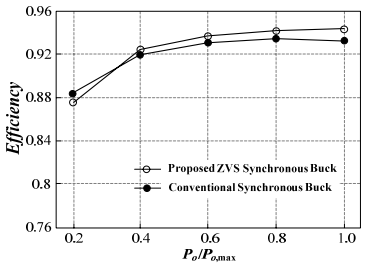


Fig. 16. Measured efficiency as a function of the output power.

Fig. 15(a)~(b) shows the key experimental waveforms of the conventional synchronous buck converter, in which the switches also use mosfet IPP530N15N3 and the output filter inductance is 200 μH as illustrated in Fig. 15(c). The main switch is hard-switching and the reverse-recovery problem of the parasitic diode of the synchronous switch is severe. The peak of reverse recovery current is high and the current change is very rapid, which induces high spike voltage across the synchronous switch. In the practical application, a RC snubber(2.5 Ω/10 nF) is employed to suppress the voltage spike, resulting in extra loss. Therefore, the conventional synchronous buck converter suffers from high switching loss as well as deteriorated EMI problem, which is effectively alleviated in the proposed ZVS converters with coupled inductors. The measured efficiency of the proposed ZVS and conventional synchronous buck converter is shown in Fig. 16. The proposed ZVS synchronous buck converter with a coupled inductor achieves a slightly lower efficiency at light load condition due to the additional conduction loss of the auxiliary circuit[5], which remains constant irrespective of the load variation according to (23). With the increased output power, the efficiency improves, reaching a maximum efficiency of 94.3% at full-load, which is nearly 1% higher than that of the conventional synchronous buck converter. Moreover, according to (23), with higher switching frequency, the average auxiliary current I_{Da} is reduced and thus the efficiency can be effectively improved at light load condition.

V. Conclusion

The topology derivation of ZVS synchronous DC-DC converters with coupled inductors which can achieve ZVS operation and eliminate the reverse-recovery problem for both switches over the whole load range, are introduced in the paper. Based on the basic cell, general ZVS topology with a coupled inductor is derived. Then systematic topology derivation is obtained with the consideration of all possible coupled inductor connections and five viable configurations are yielded for each ZVS synchronous buck, boost and buck-boost converter. Thanks to the general ZVS topology, generalized analysis suitable for these converters is performed to achieve comprehensive understanding. On the other hand, comparison is easily conducted to explore the feature of each converter and preferred converters can be chosen for different applications. Moreover, the methodology presented in the paper for topology derivation is not limited to the fundamental synchronous buck, boost and buck-boost converters, and it can revolutionize the way for other synchronous converters.

Taking the proposed ZVS synchronous buck converter in Fig. 4(e) as an example, the design considerations are addressed in detail to optimize the topology parameters and experimental results are presented to verify converter effectiveness. In the practical design, trade-off should be made between the value of turns ratio and leakage inductance in order to obtain the soft-switching merits with small voltage stress and conduction loss, as illustrated in the following:

(1) The ZVS realization and reverse-recovery problem elimination are easier with larger turns ratio and smaller leakage inductance.

(2) The voltage stress of the auxiliary diode is reduced with smaller turns ratio.

(3) The average magnetizing current and auxiliary diode current is decreased with smaller turns ratio and larger leakage inductance.

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